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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,765	07/09/2003	Chi-Yang Lin	3304.2.67	9909

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EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,765	LIN ET AL.	
	Examiner	Art Unit	
	Kee M. Tung	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The RCE and amendment filed 8/3/05 have been considered in preparing this Office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 5-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Datar et al (6,625,740 hereinafter "Datar") in view of Ellenby et al (6,064,398 hereinafter "Ellenby").

Datar teaches a method (Fig. 1 and respective areas of the specification) for accessing image data in a computer system (Fig. 1), said computer system comprising a core logic unit (combination of North bridge 103 and south bridge 110 form the system core logic chipset, col. 3, lines 6-8), a system memory (102) having an AGP memory block (it is well known that the design of Intel's AGP bus architecture is for a point-to-point connection between graphics controller and the corelogic chip to access AGP portion of system memory, normally for storing texture mapping) and a non-AGP memory block, a graphics accelerator (107), an AGP bus (106), and an image data outputting device (not shown, but would be obvious to connect to 117 and 118, col. 4, lines 10-15) in communication with a south bridge chip of said core logic unit, said method comprising receiving image data from said image data outputting device by said

core logic unit (input from 117 via PCI bus 105 to core logic unit); writing said image data directly into said AGP memory block of said system memory instead of said non-AGP memory block and accessing said image data in said AGP memory block by said graphics accelerator (inherent by the teachings of AGP bus because one of the reason to use AGP bus is for the graphics accelerator to directly access portion of the system memory, such as, AGP memory block which is usually for storing texture data). Furthermore, Ellenby teaches an image outputting device (camera 102, col. 5, lines 39-60 and col. 6, lines 12-20) connects to IEEE 1394 chipset 104 (Ellenby further teaches the invention could be implemented using other digital interfaces, now available or to be developed in the future and the USB interface has similar characteristics as the IEEE 1394 FireWire and are considered within the level of ordinary skill in the art to replace one by another, see col. 5, lines 57-60) and the chipset (104) can burst image data to anywhere in the CPU's main memory (includes the claimed AGP portion of the main memory) or to any PCI slave device's memory (col. 6, lines 12-20). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of image data outputting device of Ellenby into the system and/or method of Datar in order to receive image data from other electronic devices, such as, a camera into the image processing system for processing and thus to be able to provide a high quality image in real time. Therefore, at least claims 1-3 and 5-10 would have been obvious.

Claims 11-17 are similar in scope to claims 1-3 and 5-8, and rejected under similar rationale. Claim 11 additionally requires to determine whether said received

data is image data which would have been obvious by the teachings of chipset (104) because Ellenby teaches the chipset accepts the IEEE 1394 data from camera 102 and generates command and image data (col. 5, lines 61-67). Therefore, at least claims 11-17 would have been obvious.

3. Claims 1-3 and 5-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Datar et al (6,625,740 hereinafter "Datar") in view of or Dendinger (6,714,891).

Datar teaches a method (Fig. 1 and respective areas of the specification) for accessing image data in a computer system (Fig. 1), said computer system comprising a core logic unit (combination of North bridge 103 and south bridge 110 form the system core logic chipset, col. 3, lines 6-8), a system memory (102) having an AGP memory block (it is well known that the design of Intel's AGP bus architecture is for a point-to-point connection between graphics controller and the corelogic chip to access AGP portion of system memory, normally for storing texture mapping) and a non-AGP memory block, a graphics accelerator (107), an AGP bus (106), and an image data outputting device (not shown, but would be obvious to connect to 117 and 118, col. 4, lines 10-15) in communication with a south bridge chip of said core logic unit, said method comprising receiving image data from said image data outputting device by said core logic unit (input from 117 via PCI bus 105 to core logic unit); writing said image data directly into said AGP memory block of said system memory instead of said non-AGP memory block; and accessing said image data in said AGP memory block by said graphics accelerator (inherent by the teachings of AGP bus because one of the reason to use AGP bus is for the graphics accelerator to directly access portion of the system

memory, such as, AGP memory block which is usually for storing texture data). Furthermore, Dendinger teaches an image outputting device (digital camera, col. 7, lines 11-14) connects to a USB interface (268) and the memory controller (223/323) and bus controller (246/325) forms as the core logic unit (col. 8, lines 1-3 and col. 9, lines 26-30). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of image data outputting device of Dendinger into the system and/or method of Datar in order to receive image data from an electronic devices, such as, a camera into the image processing system for processing and thus to be able to provide a high quality image in real time. Therefore, at least claims 1-3 and 5-10 would have been obvious.

Claims 11-17 are similar in scope to claims 1-3 and 5-8, and rejected under similar rationale. Claim 11 additionally requires to determine whether said received data is image data which would have been obvious by the teachings of the digital camera (Dendinger, col. 7, line 14) because data from digital camera is considered image data to ordinary skill in the art. Therefore, at least claims 11-17 would have been obvious.

4. Claims 1-3 and 5-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US 2002/0144030) in view of Ellenby et al (6,064,398 hereinafter "Ellenby").

Miller teaches a method (Fig. 1 and respective areas of the specification) for accessing image data in a computer system (Fig. 1), said computer system comprising a core logic unit (combination of North bridge 120 and south bridge 150 form the system core logic chipset, page 2, paragraph 14), a system memory (130) having an AGP

memory block and a non-AGP memory block, a graphics accelerator (connect to AGP slot 140), an AGP bus (the bus between AGP slot and north bridge), and an image data outputting device (not shown, but would be obvious to connect to USB port 180) in communication with a south bridge chip of said core logic unit, said method comprising receiving image data from said image data outputting device by said core logic unit (input from 180 to south bridge 150); writing said image data directly into said AGP memory block of said system memory instead of said non-AGP memory block and accessing said image data in said AGP memory block by said graphics accelerator (inherent by the teachings of AGP bus because one of the reason to use AGP bus is for the graphics accelerator to directly access portion of the system memory, such as, AGP memory block which is usually for storing texture data). Furthermore, Ellenby teaches an image outputting device (camera 102, col. 5, lines 39-60 and col. 6, lines 12-20) connects to IEEE 1394 chipset 104 (Ellenby further teaches the invention could be implemented using other digital interfaces, now available or to be developed in the future and the USB interface has similar characteristics as the IEEE 1394 FireWire and are considered within the level of ordinary skill in the art to replace one by another, see col. 5, lines 57-60) and the chipset (104) can burst image data to anywhere in the CPU's main memory (includes the claimed AGP portion of the main memory) or to any PCI slave device's memory (col. 6, lines 12-20). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of image data outputting device of Ellenby into the system and/or method of Miller in order to receive image data from other electronic devices, such as, a camera

into the image processing system for processing and thus to be able to provide a high quality image in real time. Therefore, at least claims 1-3 and 5-10 would have been obvious.

Claims 11-17 are similar in scope to claims 1-3 and 5-8, and rejected under similar rationale. Claim 11 additionally requires to determine whether said received data is image data which would have been obvious by the teachings of chipset (104) because Ellenby teaches the chipset accepts the IEEE 1394 data from camera 102 and generates command and image data (col. 5, lines 61-67). Therefore, at least claims 11-17 would have been obvious.

5. Claims 1-3 and 5-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US 2002/0144030) in view of Dendinger (6,714,891).

Miller teaches a method (Fig. 1 and respective areas of the specification) for accessing image data in a computer system (Fig. 1), said computer system comprising a core logic unit (combination of North bridge 120 and south bridge 150 form the system core logic chipset, page 2, paragraph 14), a system memory (130) having an AGP memory block and a non-AGP memory block, a graphics accelerator (connect to AGP slot 140), an AGP bus (the bus between AGP slot and north bridge), and an image data outputting device (not shown, but would be obvious to connect to USB port 180) in communication with a south bridge chip of said core logic unit, said method comprising receiving image data from said image data outputting device by said core logic unit (input from 180 to south bridge 150); writing said image data directly into said AGP memory block of said system memory instead of said non-AGP memory block and

accessing said image data in said AGP memory block by said graphics accelerator (inherent by the teachings of AGP bus because one of the reason to use AGP bus is for the graphics accelerator to directly access portion of the system memory, such as, AGP memory block which is usually for storing texture data). Furthermore, Dendinger teaches an image outputting device (digital camera, col. 7, lines 11-14) connects to USB interface (268) and the memory controller (223/323) and bus controller (246/325) forms as the core logic unit (col. 8, lines 1-3 and col. 9, lines 26-30). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of image data outputting device of Dendinger into the system and/or method of Datar in order to receive image data from an electronic devices, such as, a camera into the image processing system for processing and thus to be able to provide a high quality image in real time. Therefore, at least claims 1-3 and 5-10 would have been obvious.

Claims 11-17 are similar in scope to claims 1-3 and 5-8, and rejected under similar rationale. Claim 11 additionally requires to determine whether said received data is image data which would have been obvious by the teachings of the digital camera (Dendinger, col. 7, line 14) because data from digital camera is considered image data to ordinary skill in the art. Therefore, at least claims 11-17 would have been obvious.

Response to Arguments

6. Applicant's arguments filed 4/25/05 and 8/3/05 have been fully considered but they are not persuasive.

Regarding arguments from 8/3/05 to Peddada, at the first, applicant argues that there is no relevant description disclosing that the image data is directly stored into the AGP memory block of system memory without transference of the image data inside the system memory except the dashed arrow flowing from the disc 18 to AGP memory 14 in Fig. 5. Well, this obviously is relevant enough to support that the image data is directly transferred from disc 18 to AGP memory 14 since the dashed arrow is not point to other portion of main memory and then direct to the AGP portion of memory. Then, applicant argues that the bus used in Peddada is a PCI bus where the claims required an USB interface. Newly cited prior art to Zumkehr proves that an USB bus, AGP bus, PCI bus and other I/O bus are interchangeable to one of ordinary skill in the art.

Regarding arguments from 4/25/05, Basically, applicant argues that none of the cited references disclose or suggest that the image data is directly written into the AGP memory block of the system memory instead of the non-AGP memory block of the system memory and it is ***still possible*** that the image data is not directly written into the AGP memory block. The examiner disagrees. It is well known in the graphics art that some times the system memory is divided into two portions. One is used by the CPU and called processor memory (just the normal system memory) is exclusively used by the processor, another portion of the system memory is allocated for graphics accelerator and is normally called graphics memory portion or AGP memory block. The graphics/image data is only allowed to store in this portion of the system memory. The size of this AGP memory block normally can be dynamically allocated. Therefore, in response to applicant's argument, the image data in the cited references is directly

stored into the AGP memory block instead of the non-AGP memory block because it is not allowed by the processor.

Regarding arguments to Datar, applicant argues that Datar teaches an AGP bus 106, but fails to disclose or suggest an AGP memory block and a non-AGP memory block. As well known in the art ever since the Intel's AGP bus architecture, the purpose of the AGP bus is for the graphics accelerator to access the AGP portion of main memory directly because the AGP bus is a point-to-point directed connection. Therefore, it is inherently that if there is an AGP bus, there is an AGP memory in the main memory (check out Intel's AGP specification). Then, applicant argues that "the examiner acknowledges that Datar fails to disclose the claimed step of "writing said image data .... of said non-AGP memory block". Well, the examiner never acknowledges because the feature is an inherent feature in view of AGP architecture of Datar as detailed above. Datar never teaches or suggest the image data is writing into the non-AGP portion of main memory and then transfer to the AGP portion of main memory. Furthermore, in memory art, accessing memory usually means both "writing" into and "reading" from the memory.

Regarding arguments to Ellenby or Dendinger, it is noted that the examiner used Ellenby or Dendinger for the teachings of image output device. Applicant cannot show non-obviousness by attacking references individually where, as here the rejections are based on combination of references.

Regarding arguments to Miller, applicant argues that Miller also fails to teach AGP and non-AGP memory block, but does teach AGP slot 140. See above response

regarding Datar's AGP bus for similar response and inherent features of AGP architecture.

Therefore, applicant's arguments are not deemed to be persuasive.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Peddada et al (6,295,068) teaches image/texture data is copied or transferred from disk 18 to AGP memory 14 of main memory over PCI bus 28 (Fig. 5).

Zumkehr et al (2003/0235086) teaches PCI bus, AGP bus, USB bus and other I/O bus are interchangeable to one of ordinary skill in the art (par 0010).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M. Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2671